# SY7T625

## Isolated Metrology Processor for Electricity Metering Applications

## General Description

The SY7T625 is the host side device of an isolated metering chipset for single-phase or poly-phase electricity metering applications. Featuring Silergy's proprietary Teridian power measurement technology, up to four isolated analog front end (AFE) devices are supported, each utilizing an independent, robust capacitively coupled digital interface. Each AFE supports two ADC channels (voltage and current) to form a highly accurate and fully isolated shunt-based meter.

A powerful 24-bit Compute Engine and math accelerators implement the core requirements of high accuracy metering. Code images that cover most requirements of revenue metering are provided by Silergy. These images can be pre-loaded into the flash memory of the SY7T625 by ordering option, programmed at production, and can be updated in the field, if necessary. The flash memory is also used to store calibration coefficients generated during meter calibration and configuration.

Designed as a completely autonomous metrology processor, a set of pre-processed metrology outputs can be obtained by reading registers via the SPI interface. Likewise, system parameters, such as the desired meter constant (Kh), calibration coefficients, sag threshold, and other parameters can be written to RAM by the host.

A sophisticated onboard clock management system provides an internal clock source and automatically utilizes an optional external crystal if the highest accuracy timing is desired. An integrated hardware Watchdog Timer (WDT) is also included.

The example schematic illustrates an application of four SY7M007 isolated AFEs connected to voltage and current sensors for each phase. Scaled voltages from the sensors are digitized, and the data stream of measurement data is coupled to the SY7T625 with discrete or PCB capacitors.

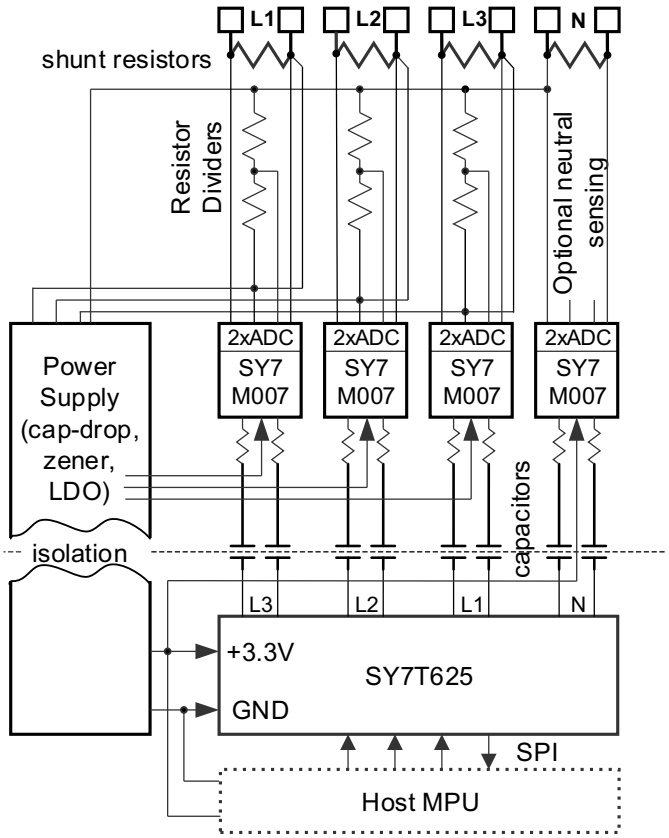


## Features

- Isolated AFE interface supports up to four compatible Silergy remote ADCs (up to 8 analog inputs)
- Powerful 24-bit Compute Engine with 20MHz clock frequency, supported by accelerators for multiply, divide, and square root operations
- Factory-programmed or field programmable with Silergy provided firmware images
- 5x5mm 32-pin QFN package
- SPI host interface, up to 10MHz
- Two pulse outputs and 10 additional digital I/O pins
- 20MHz crystal (or external clock) interface for precision timing reference

## Applications

- Poly-phase smart meters
- Industrial meters

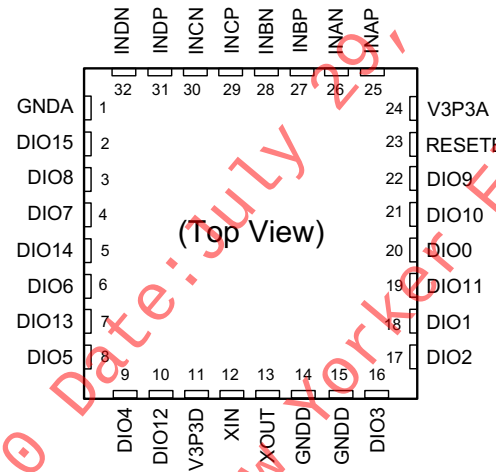


## Ordering Information

| Ordering Number | Pre-programmed Firmware | Package | Top Mark |
|---|---|---|---|
| SY7T625T | None (internal flash must be erased and Silergy-provided firmware must be installed by the OEM) | QFN5x5-32<br>Tape and reel carrier<br>RoHS Compliant and Halogen Free | SY7T625<br>RRYYWWZ |
| SY7T625T+MTR | Internal flash contains standard meter firmware | | |

*RR=Die revision code, YY=year (2 digits) of assembly, WW=work week of assembly, Z= lot code*

## Pinout



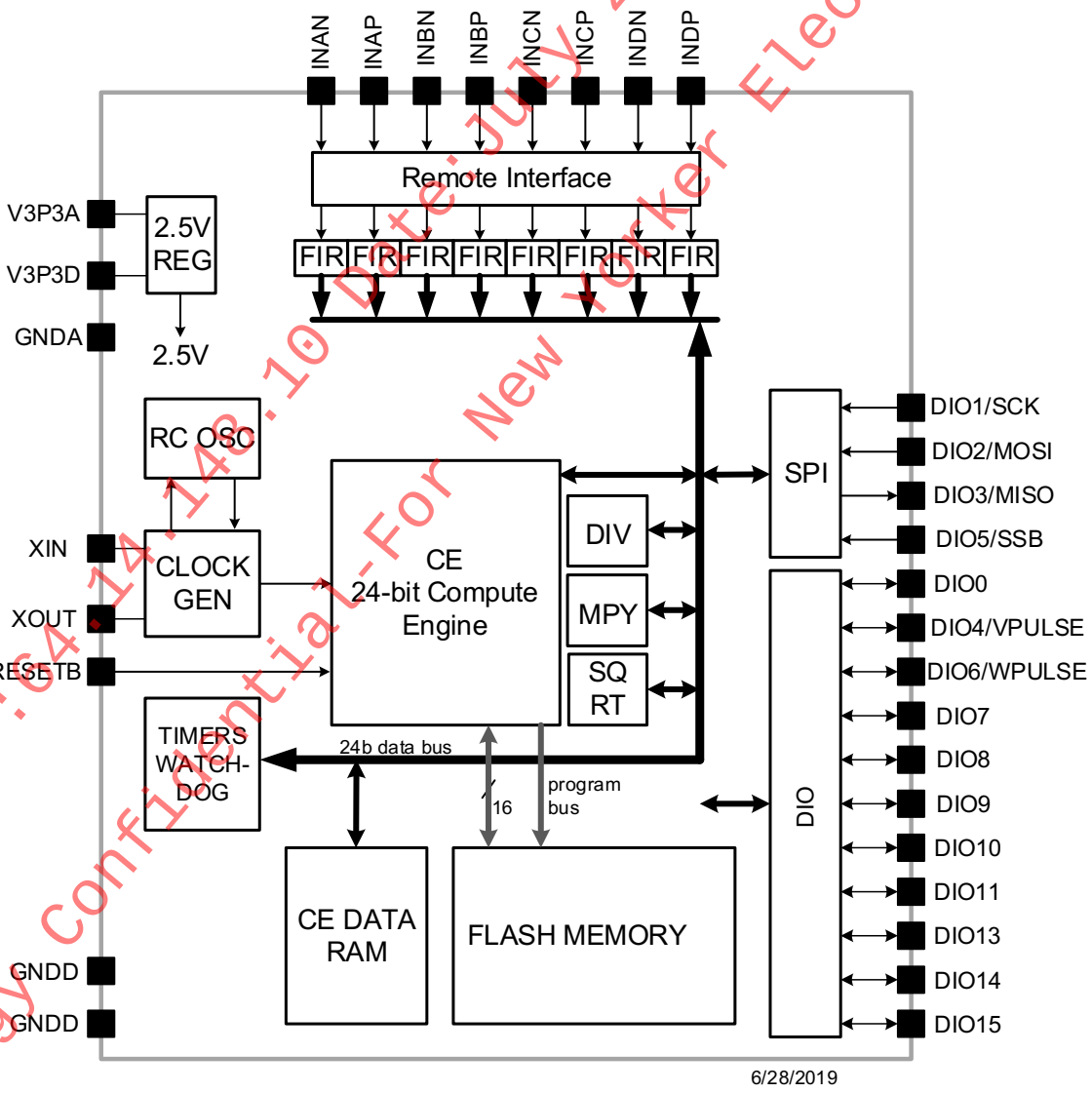

| Pin | Signal | Function | Pin | Signal | Function |
|---|---|---|---|---|---|
| 1 | GNDA | Analog GND | 17 | DIO2 | SPI MOSI (SDI) |
| 2 | DIO15 | Digital I/O | 18 | DIO1 | SPI SCK |
| 3 | DIO8 | Digital I/O | 19 | DIO11 | Digital I/O |
| 4 | DIO7 | Digital I/O | 20 | DIO0 | Digital I/O |
| 5 | DIO14 | Digital I/O | 21 | DIO10 | Digital I/O |
| 6 | DIO6 | Digital I/O or Wh pulse output | 22 | DIO9 | Digital I/O |
| 7 | DIO13 | Digital I/O | 23 | RESETB | Reset Input (Active Low) |
| 8 | DIO5 | SPI Select SSB | 24 | V3P3A | 3.3VDC Supply (Analog) |
| 9 | DIO4 | Digital I/O or VARh pulse output | 25 | INAP | Remote Interface A (positive) |
| 10 | DIO12 | Digital I/O | 26 | INAN | Remote Interface A (negative) |
| 11 | V3P3D | 3.3VDC Supply (Digital) | 27 | INBP | Remote Interface B (positive) |
| 12 | XIN | Crystal Oscillator Input | 28 | INBN | Remote Interface B (negative) |
| 13 | XOUT | Crystal Oscillator Output | 29 | INCP | Remote Interface C (positive) |
| 14 | GNDD | Ground (Digital) | 30 | INCN | Remote Interface C (negative) |
| 15 | GNDD | Ground (Digital) | 31 | INDP | Remote Interface D (positive) |
| 16 | DIO3 | SPI MISO (SDO) | 32 | INDN | Remote Interface D (negative) |
| 33 | -- | Metal pad on bottom – N/C | | | |

# 1. Hardware Description

The SY7T625 integrates all the functional hardware blocks required for solid-state electricity metering. Only a few external resistors and capacitors are required. Included on the device are:

- Remote (Rx) interface for capacitive coupling to remote ADCs
- Two FIRs per remote
- 24-bit Compute Engine with RAM and Flash memory
- Digital I/O with SPI peripheral interface and low jitter pulse outputs
- Oscillator and clock management logic
- Integrated power-on reset and watchdog timer

## 1.1 SY7T625 Functional Block Diagram



## 1.2 Clock Management, Power-On Reset, and Watchdog Timer

**Clock Management**

The SY7T625 integrates an RC oscillator for fast start-up and includes the circuitry to handle an external crystal or ceramic resonator. The clock management unit of the SY7T625 automatically handles the clock sources logic and distributes the clock to the rest of the device.

Upon reset or power-on, the SY7T625 starts-up on the internal RC oscillator. After 1024 clock cycles of the internal RC oscillator, the clock management logic will switch to the external 20MHz clock (if available), allowing the external crystal an adequate start-up time. If no valid external clock is detected, the clock management logic will keep clocking the device using the internal RC oscillator. If the device is normally clocked using the external 20MHz crystal, the clock management logic continuously monitors the status of the clock. The clock management logic of the SY7T625 will automatically switch to the internal oscillator in the event of a failure of the external oscillator (or crystal not mounted).

The internal RC oscillator is trimmed and provides an accurate clock source, however for metering applications requiring highest accuracy of the time-based measurements (i.e. line frequency, energy, etc.), the use of an external crystal is required. Alternatively, an external clock signal can be utilized instead of the crystal. In this case, the external clock should be connected to the XOUT pin while the XIN pin should be connected to GNDD.

**Power-On Reset (POR)**

An on-chip Power-On Reset (POR) block monitors the supply voltage (V3P3D) and initializes the internal digital circuitry at power-on. Once V3P3D is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It will also issue a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

**External Reset Pin (RESETB Pin)**

In addition to the internal reset sources, a reset can be forced by applying a low level to the RESETB pin for a duration of > Tspike (MAX) (see the Transient Spike Tolerance specification in the Electrical Characteristics section of this document).

If the RESETB pin is pulled low, all digital activities in the device stop, except the clock management circuitry and oscillators, which continue to run.

**Watchdog Timer (WDT)**

A Watchdog Timer (WDT) block detects any software processing errors. The embedded firmware periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated.

## 1.3 Isolated (Remote ADC) Interface

The SY7T625 communicates with one or more remote ADCs (e.g. the SY7M007 dual-channel remote ADC) via capacitive isolation. The communication protocol is proprietary. Below are a few characteristics of the data link:

- Data are sent exclusively from the remote ADCs to the SY7T625 host. Neither commands nor data are sent in the opposite direction.
- Differential signaling is used for best rejection of common-mode noise. Every remote drives two signals, RCP and RCN with approximately 3.2V peak amplitudes. Depending on the value of the coupling capacitor, the peak voltage received at the SY7T625 can be as low as 50mV (66mV typical with 0.2pF PCB capacitors interacting with 10pF trace/pin capacitance in the SY7T625).
- Manchester encoding is used to ensure that there is no DC component to the signal and that the clock can be recovered by the SY7T625.
- The half-bit bit-time is 10MHz, or 100ns. Each full bit occupies 200ns.
- The ADC sample data generated by the sigma-delta comparator stage in the remote ADCs is transmitted in the form of a bit stream to the host and decimated via FIR filters in the SY7T625.
- ADC sample data and auxiliary data such as die temperature, supply voltage, trim information, etc. are sent in ‘data frames’ of 7 bits to the SY7T625 host. Each frame contains 4 bits for synchronization, one bit each for the current and the voltage samples, and one side-channel bit. Each data frame occupies 1.4µs.

- The ADC sample data are transmitted to the SY7T625 sequentially and matched to factory programmed periods for chopping of the bandgap reference. Factory-programmable settings of the FIR filters in the SY7T625 allow various combinations of effective sample frequency and resolution.
- Timing for a typical application assumes that 170 bits are collected for one complete 'multiplexer frame', resulting in a mux frame time of 170 * 1.4µs = 238µs (4201.68Hz).
- The polarity of the signals at the INAP/INAN, INBP/INBN, etc. pins of the SY7T625 can be swapped to accommodate signal routing on the PCB.

The design of the remote communication link is optimized for two distinct capacitance values. The capacitors can be implemented in two ways:

1) Discrete capacitors, 100pF, in series with 200kΩ resistors
2) PCB capacitors, 0.2pF (4mm x 4mm and 2mm x 2mm copper plates on opposing sides of a 1.6mm thick PCB), in series with 2kΩ resistors

A configuration bit in the SY7T625 matches the remote interface to the selected capacitor configuration. Minor differences in the capacitance values and the capacitive load from traces and input pins of the SY7T625 for the two capacitors for each remote link can be balanced using bit fields that are accessible through the SPI interface (see the CE Code Reference Manual for details). Common-mode values read from the remote pin pairs are accessible via one register per remote channel.

## 1.4 Compute Engine

The Compute Engine is a dedicated 24-bit DSP that performs the signal processing necessary to accurately measure energy. The Compute Engine is a programmable core for which Silergy typically provides binary code modules used to perform energy computations. The CE calculations and processes may include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time)
- 90° phase shifter (for VAR calculations)
- Pulse generation
- Measurement of the input signal frequency (for frequency and phase information)
- Monitoring of the input signal amplitude (for sag detection)
- Scaling of the processed samples based on calibration coefficients
- Scaling of samples based on temperature compensation information
- Extraction, suppression or filtering of harmonics for special functions
- Variable gain compensation
- Variable phase compensation

## 1.5 Flash and RAM

The SY7T625 includes on-chip flash memory for storing program code, coefficients, calibration data, and configuration settings. The SY7T625 also includes on-chip RAM which is used to store the values of input and output registers and utilized by the firmware for its operations.

## 1.6 Digital I/O

The SY7T625 features general-purpose digital I/O. The digital I/O are either managed directly by the user, by the embedded firmware, or multiplexed with the serial communication interfaces. The following table summarizes the multiplexing and pin assignment on the SY7T625.

| Pin Name | Pin # | Hardware Peripheral | Pin Name | Pin # | Hardware Peripheral |
|---|---|---|---|---|---|
| DIO15 | 2 | | DIO7 | 4 | |
| DIO14 | 5 | | DIO6 | 6 | W Pulse |
| DIO13 | 7 | | DIO5 | 8 | SSB |
| DIO12 | 10 | | DIO4 | 9 | V Pulse |
| DIO11 | 19 | | DIO3 | 16 | MISO |
| DIO10 | 21 | | DIO2 | 17 | MOSI |
| DIO9 | 22 | | DIO1 | 18 | SCK |
| DIO8 | 3 | | DIO0 | 20 | |

## 1.7 Serial Peripheral Interface (SPI)

SPI transactions work in two selectable modes:

- Native SY7T625 SPI operation mode (operation up to 1MHz)
- MAX71020-style SPI operation mode (operation up to 10MHz)

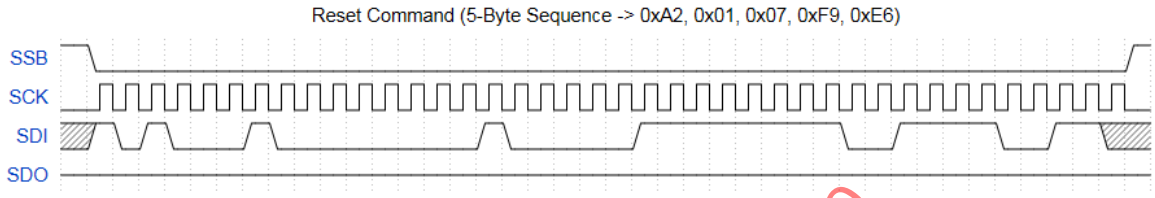
The code image provided by Silergy determines the SPI operation mode. In MAX71020-style SPI operation mode, SPI transactions are configured to provide immunity to electrical noise through redundancy in the command segment and error checking in the data field. The SY7T625 SPI transaction is exactly 64 bits (none of the fields are optional).

- Transactions of any other length are rejected and if an error is detected during the address or direction phase, no action is taken
- If extra clocks are provided at the end during a read, all zero is output and the status continues to be updated, signaling an error.
- If extra clocks are provided at the end during a write, the write is aborted, and the status is updated to signal an error.
- The status byte indicates the status of the previous SPI transaction except for the status byte parity.
- Access to the entire address range is allowed, unless Safe Mode is selected, which restricts access to the first 256 RAM locations (0x00 to 0xFF).

### 1.7.1 Reset Command

The reset command works identical for both SY7T625-style and MAX71020-style SPI modes. It is a 5-byte sequence (0xA2, 0x01, 0x07, 0xF9, 0xE6) issued by the host SPI master. The last bit of this 5-byte sequence is a don't-care bit.

| Byte Number | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 3 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 4 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 5 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | x |




### 1.7.2 Single-Word SPI Reads

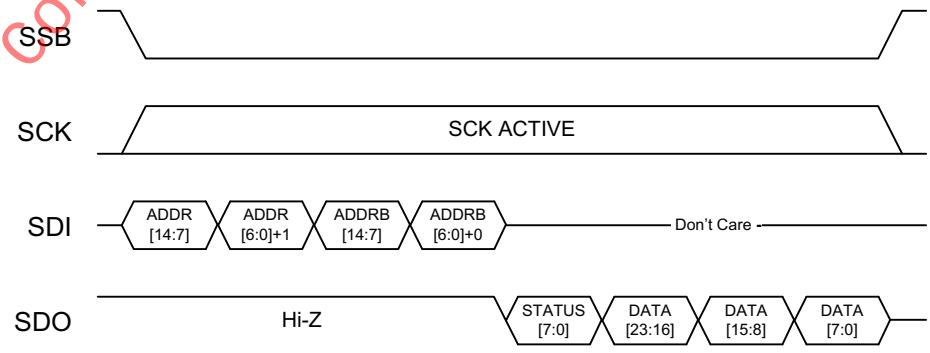
The read command from the host SPI master uses the target address (ADDR) and the inverted target address (ADDRB) for added security:

| Byte Number | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | ADDR[14:7] | | | | | | | |
| 2 | ADDR[6:0] | | | | | | | 1 |
| 3 | ADDRB[14:7] | | | | | | | |
| 4 | ADDRB[6:0] | | | | | | | 0 |
| 5 | x | x | x | x | x | x | x | x |
| 6 | x | x | x | x | x | x | x | x |
| 7 | x | x | x | x | x | x | x | x |
| 8 | x | x | x | x | x | x | x | x |

Note 'x' means bit is a don't-care bit.

Response from SY7T625 SPI slave:

| Byte Number | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Hi-Z | | | | | | | |
| 2 | Hi-Z | | | | | | | |
| 3 | Hi-Z | | | | | | | |
| 4 | Hi-Z | | | | | | | |
| 5 | STATUS[7:0] | | | | | | | |
| 6 | DATA[23:16] | | | | | | | |
| 7 | DATA[15:8] | | | | | | | |
| 8 | DATA[7:0] | | | | | | | |



### 1.7.3 Single Word SPI Write

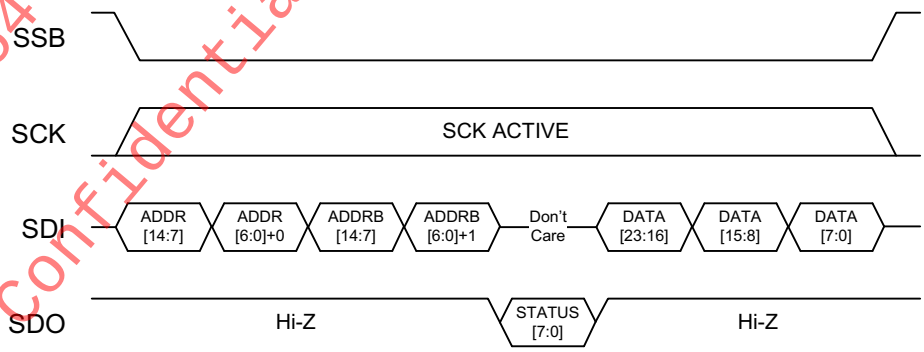
Write command from host SPI master (ADDR = target address, ADDRB = target address with bits reversed):

| Byte Number | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | ADDR[14:7] | | | | | | | |
| 2 | ADDR[6:0] | | | | | | | 0 |
| 3 | ADDRB[14:7] | | | | | | | |
| 4 | ADDRB[6:0] | | | | | | | 1 |
| 5 | x | x | x | x | x | x | x | x |
| 6 | DATA[23:16] | | | | | | | |
| 7 | DATA[15:8] | | | | | | | |
| 8 | DATA[7:0] | | | | | | | |

Note 'x' means that the bit is a don't-care bit.

Response from SY7T625 SPI slave:

| Byte Number | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | Hi-Z | | | | | | | |
| 2 | Hi-Z | | | | | | | |
| 3 | Hi-Z | | | | | | | |
| 4 | Hi-Z | | | | | | | |
| 5 | STATUS[7:0] | | | | | | | |
| 6 | Hi-Z | | | | | | | |
| 7 | Hi-Z | | | | | | | |
| 8 | Hi-Z | | | | | | | |



### 1.7.4 Status Byte

Even parity is used for both data and status parity.

| Bit | Name | Description |
|---|---|---|
| 7 | Status Parity | Parity of the status byte, STATUS [7:0] ('0' or '1' could be correct) |
| 6 | FIFO Overrun | SPI FIFO overrun error ('1' signifies error) |
| 5 | FIFO Underrun | SPI FIFO underrun error ('1' signifies error) |
| 4 | Data Parity | Parity of the data word, DATA [23:0] ('0' or '1' could be correct) |
| 3 | Setting Mismatch | Address or direction mismatch error ('1' signifies error) |
| 2 | (Reserved) | |
| 1 | Bad Clock Count | Bit count not equal to 64 error ('1' signifies error) |
| 0 | Bad Address | Address out of bounds, when in SPI Safe Mode |

# 2 Electrical Specifications

## 2.1 Absolute Maximum Ratings (1)

| | |
|---|---|
| **Supplies and Ground Pins:** | |
| V3P3D, V3P3A | -0.5V to 3.8V |
| GNDD, GNDA | -0.5V to +0.5V |
| **Crystal Pins:** | |
| XIN, XOUT | -10mA to +10mA<br>-0.5V to 3.0V |
| **Digital Pins:** | |
| DIO15, DIO14, DIO13, DIO12, DIO11, DIO10, DIO9, DIO8, DIO7, DIO6, DIO5, DIO4, DIO3, DIO2, DIO1, DIO0 | -10mA to +10mA<br>-0.5V to (V3P3D + 0.5V) |
| **Receiver Input Pins:** | |
| INAN, INAP, INBN, INBP, INCN, INCP, INDN, INDP | -10mA to +10mA<br>-0.5V to (V3P3A + 0.5V) |
| **Temperatures:** | |
| Operating Junction Temperature (peak, 100ms) | +140°C |
| Operating Junction Temperature (continuous) | +125°C |
| Storage Temperature | -45°C to +165°C |
| Soldering Temperature (10-second duration) | +250°C |
| ESD Stress on All Pins | ±2kV |

## 2.2 Recommended Operating Conditions (2)

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| 3.3V Supply Voltage (V3P3) | Normal Operation | 3.0 | 3.3 | 3.6 | V |
| Operating Temperature | | -40 | – | +85 | ºC |

## 2.3 Recommended External Components

| Name | From | To | Function | Value | Unit |
|---|---|---|---|---|---|
| $C_D$ | V3P3D | GNDD | Bypass capacitor for V3P3D | 0.1±20% | µF |
| $C_A$ | V3P3A | GNDA | Bypass capacitor for V3P3A | ≥1.0±30% | µF |
| XTAL | XIN | XOUT | 20MHz crystal | 20.000 | MHz |
| CXS | XIN | GNDD | Load capacitor values for crystal depend on crystal specifications and board parasitics. Nominal values are based on 4pF board capacitance and include an allowance for chip capacitance. | 20 ±10% | pF |
| CXL | XOUT | GNDD | | 20 ±10% | pF |

## 2.4 Performance Specifications (3)

Note that production tests are performed at room temperature.

### 2.4.1 Input Logic Levels (Digital Pins)

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Digital high-level input voltage, $V_{IH}$ | | 0.65 * V3P3D | – | – | V |
| Digital low-level input voltage, $V_{IL}$ | | – | – | 0.35 * V3P3D | V |
| Hysteresis | | 0.1 * V3P3D | – | – | V |
| Input Pull-Up Resistor $R_{PUP}$ | | 20 | – | 100 | kΩ |
| Input High Current $I_{IH}$ | Input Pull-Up Resistor Disabled | – | – | +1 | µA |
| Input Low Current $I_{IL}$ | | -1 | – | – | µA |

### 2.4.2 Input Analog Levels (Remote Receivers)

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Bias Voltage | $V_{cm}$ = open, *R2K_EN* = 1 | 1.79 | 1.82 | 1.86 | V |
| Differential Input Resistance | $V_{cm}$ = 1.8V, $V_{in}$ = ±100mV, *R2K_EN* = 1 | | 4.2 | | kΩ |
| | $V_{cm}$ = 1.8V, $V_{in}$ = ±100mV, *R2K_EN* = 0 | | 162 | | |
| Input Voltage Offset | $V_{cm}$ = 0V | -7 | | +7 | mV |
| | $V_{cm}$ = 1.8V | -5.5 | | +5.5 | mV |
| | $V_{cm}$ = V3P3A | -7 | | +5.1 | mV |

### 2.4.3 Output Logic Levels

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Digital high-level output voltage $V_{OH}$ | $I_{LOAD}$ = 1mA | V3P3D - 0.1 | – | – | V |
| | $I_{LOAD}$ = 10mA | V3P3D - 0.7 | – | – | V |
| Digital low-level output voltage $V_{OL}$ | $I_{LOAD}$ = -1mA | 0 | – | 0.1 | V |
| | $I_{LOAD}$ = -10mA | – | – | 0.5 | V |

### 2.4.4 Supply Current

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{3P3D}$ current | Normal Operation (all remote channels disabled) | – | 2.0 | 5.0 | mA |
| $V_{3P3A}$ current | | – | 9.9 | 11.5 | mA |
| Additional $V_{3P3A}$ Operating Current | Normal Operation (only one remote channel enabled) | | 0.7 | 0.9 | mA |
| Additional $V_{3P3D}$ Operating Current | | | 0.4 | 0.6 | mA |
| Additional $V_{3P3A}$ Operating Current | Normal Operation (all remote channels enabled) | | 1.9 | 2.4 | mA |
| Additional $V_{3P3D}$ Operating Current | | | 1.6 | 1.8 | mA |

### 2.4.5 Internal RC Oscillator

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Nominal Frequency | V3P3 = 3.3V, 25ºC | – | 20.000 | – | MHz |
| Accuracy | | -2 | | +2 | % |

### 2.4.6 External Crystal Oscillator

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Nominal Frequency | | – | 20.000 | – | MHz |
| Transconductance | | 1.3 | – | – | mS |
| Peak Output Source Current | Startup with XIN = XOUT = 0V, -40°C to +85°C | 950 | | 1250 | µA |
| | XIN = 1V peak, 20MHz | 0.58 | | 1.45 | mA |

## 2.5 Timing Specifications

### 2.5.1 SPI Slave Port

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Setup time from fall of SSB to rise of SCK | Tssu | 10 | | | ns |
| Setup time for SDI to rise of SCK | Tsu | 10 | | | ns |
| Hold time for SDI to rise of SCK | Thd | 10 | | | ns |
| Delay of SDO from fall of SCK | Td | | | 40 | ns |
| Hold time from rise of SCK to rise of SSB | Tshd | 15 | | | ns |
| Period of SCK | Tper | 100 | | | ns |
| Duration of SCK high state | Thi | 50 | | | ns |
| Duration of SCK low state | Tlo | 50 | | | ns |
| Bus Idle (Free) time between transactions (time from rise of SSB to next fall of SSB) | Tbuf | 250 | | | ns |

## 2.6 Reset Specifications

### 2.6.1 Power-On Reset Voltage Thresholds

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POR Release Threshold | V3P3A rising until reset is released | | | 1.76 | V |
| POR Assertion Threshold | V3P3A falling until reset is asserted | 1.56 | | | |

### 2.6.2 Transient Spike Tolerance

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RESETB Tspike† | Negative going Spike | 300 | 600 | 1050 | ns |

† When RESETB is asserted low, it must be held low at least Tspike (MAX) duration to assert a reset. Pulses narrower than Tspike (MIN) will be ignored.

## 2.7 Flash Memory Specifications

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Write Cycles Endurance | | 20,000 | | | Cycles |
| Data Retention | $T_A$ = 25°C | 100 | | | Years |
| Data Retention | $T_A$ = 85°C | 25 | | | Years |
| Page Erase Time | | 4 | | 6 | ms |
| Mass Erase Time | | 20 | | 40 | ms |
| Write Time (Word Program Time) | | 6 | | 7.5 | µs |

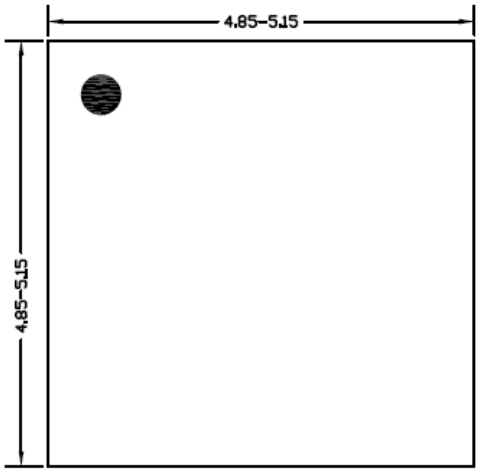
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The device is not guaranteed to function outside its operating conditions.

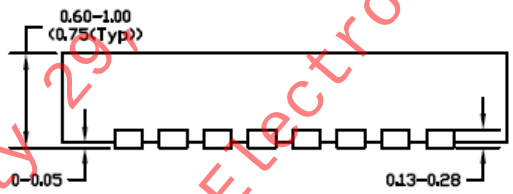
Note 3: Production testing is performed at 25°C; limits at -40°C to +85°C are guaranteed by design, test or statistical correlation.

# 3 Mechanical Dimensions, PCB Layout, and Packaging Information

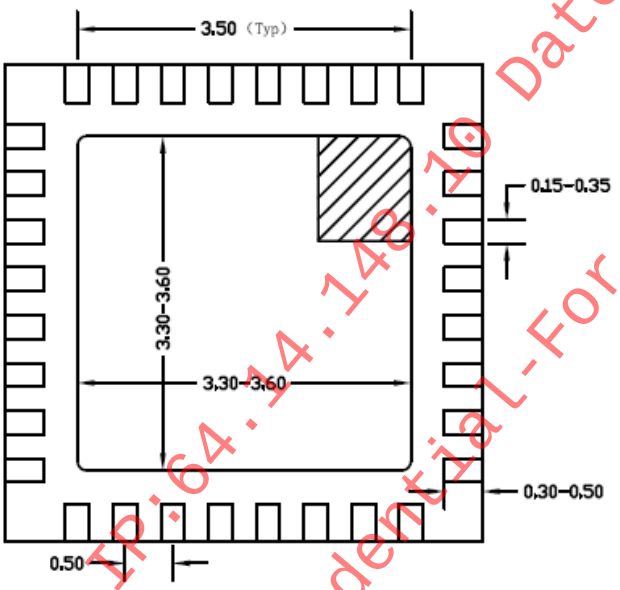
## 3.1 Mechanical Dimensions



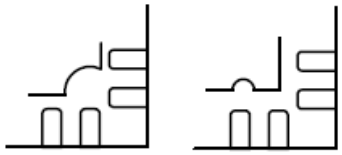

Top View




Side View



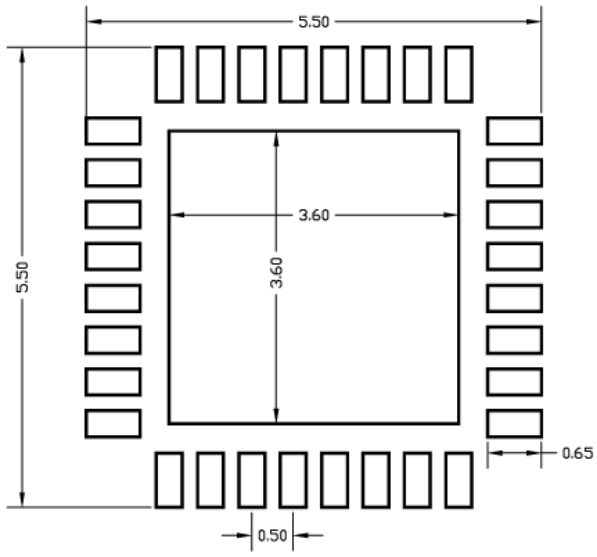

Bottom View



Detail A
Pin1 Identifier: two options

**Note: All dimensions are in mm and exclude mold flash and metal burr.**

## 3.2 PCB Layout

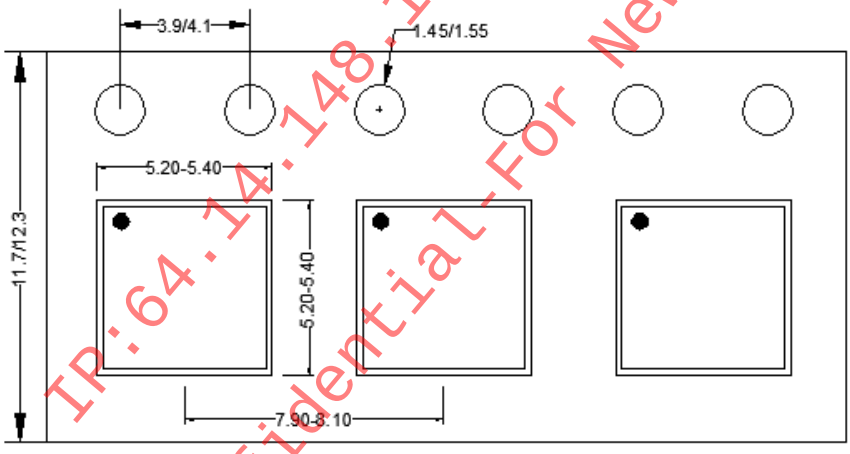



**PCB Layout (reference only)**

## 3.3 Tape & Reel Orientation

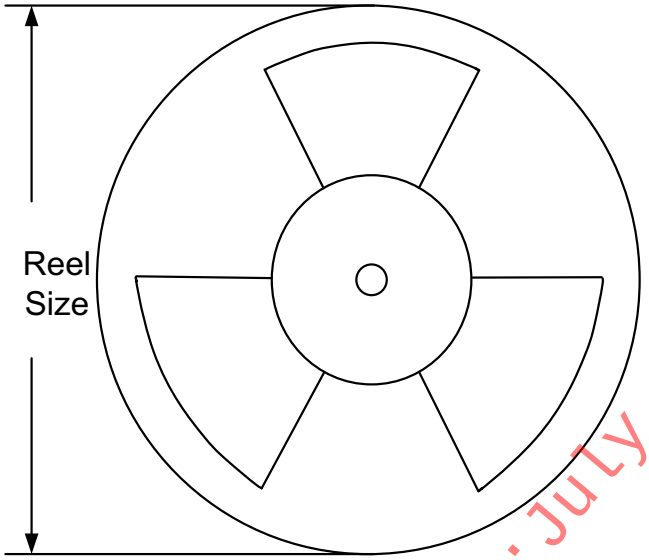
### 3.3.1 Taping Orientation

**QFN5x5-32**




**Feeding Direction**

### 3.3.2 Carrier Tape & Reel Specification for Packages




| Package type | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length (mm) | Leader length (mm) | Qty per reel (pcs) |
|---|---|---|---|---|---|---|
| QFN5x5-32 | 12 | 8 | 13" | 400 | 400 | 5000 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0.9 | 6/8/2020 | Initial release | All |
| | | | |
| | | | |

Revision history is for reference only and may not be comprehensive or complete.

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